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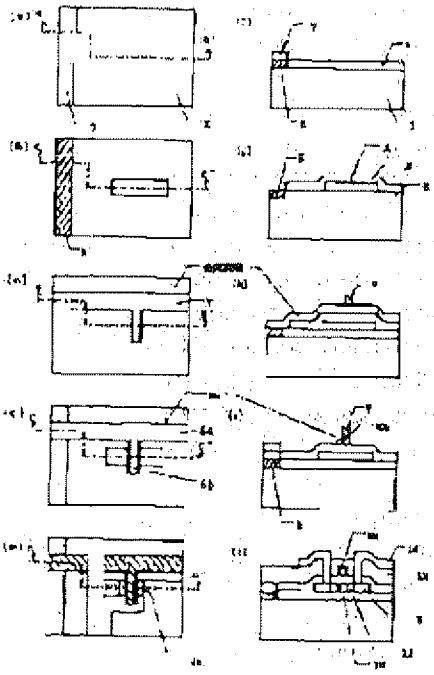
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a manufacturing method which does not damage characteristics and yield of an element when a thin film transistor having an offset region is manufactured, and provide the structure of the thin film transistor and the peripheral wiring.
SOLUTION: By selectively oxidizing a metal thin film deposited on an insulating substrate 1, a metal oxide film 2 is formed, on which a thin film transistor is formed. The part left in the state of the metal thin film which is not oxidized is electrically connected with a wiring connected with the thin film transistor or one end of an electrode. The part left in the state of the metal thin film is made a voltage applying terminal when an anodic oxidation film 8b is formed around a gate electrode 6b of the thin film transistor. A plurality of thin film transistors wherein anodic oxidation films are formed around the gate electrodes are mutually electrically connected via intermediate electrodes formed of the parts left in the state of the metal thin film.



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CLAIMS

[Claim(s)]
[Claim 1]A semiconductor device which is provided with the following and characterized by electrically connecting this thin film transistor to said metal electrode.
A metallic oxide film field which oxidized selectively and formed a metal thin film formed on a

substrate which has an insulation surface.
A metal electrode formed in said some of metal thin films.
Two or more thin film transistors formed on said metallic oxide film.

[Claim 2]A semiconductor device which is provided with the following and characterized by electrically connecting a gate electrode of this thin film transistor, or an end of a gate wire to said metal electrode, and this metal electrode being a voltage impressing terminal at the time of anodizing a gate electrode or a gate wire of said thin film transistor.
A metallic oxide film field which oxidized selectively and formed a metal thin film formed on a substrate which has an insulation surface.
A metal electrode formed in said some of metal thin films.
Two or more thin film transistors formed on said metallic oxide film.

[Claim 3]A semiconductor device of an application for patent, wherein an anodization control means which is some of said gate electrodes or gate wires, and controls advance of anodization of said gate electrode or a gate wire in a position of said voltage impressing terminal slippage is established given in the 2nd paragraph of a range.
[Claim 4]A semiconductor device of an application for patent, wherein the 2nd voltage impressing terminal that estranged with said voltage impressing terminal and was formed is electrically connected with said gate wire in a position of said thin film transistor slippage rather than this anodization control means given in the 3rd paragraph of a range.
[Claim 5]A metallic oxide film field which oxidized selectively and formed a metal thin film formed on a substrate which has an insulation surface, Have a metal electrode formed in said some of metal thin films, and two or more thin film transistors formed on said metallic oxide film, and At least one of a source electrode of one thin film transistor in this thin film transistor, or the drain electrodes A semiconductor device, wherein a gate electrode of other thin film transistors is electrically connected by relay electrode by said metal electrode.
[Claim 6]The 1st paragraph of a range of an application for patent thru/or a semiconductor device given in the 5th paragraph, wherein said metal thin film is metal in which anodization or thermal oxidation is possible and said metallic oxide film is an oxide film on anode or an oxidizing film by metal in which this anodization or thermal oxidation is possible.
[Claim 7]A manufacturing method of a semiconductor device characterized by comprising the following.
A process of depositing a metal thin film on a substrate which has an insulation surface.
A process of making a partial area of this metal thin film remaining in the state of a metal thin film; oxidizing other fields, and forming a metallic oxide film.
A process of forming a thin film transistor on this metallic oxide film.
A process which electrically connects an electrode connected to this thin film transistor, or an end of wiring to a field made to remain in the state of said metal thin film.

[Claim 8]A manufacturing method of a semiconductor device characterized by comprising the following.
A process of depositing a metal thin film on a substrate which has an insulation surface.
A process of making a partial area of this metal thin film remaining in the state of a metal thin film, oxidizing other fields, and forming a metallic oxide film.
A process of forming a thin film transistor on this metallic oxide film.
A process which electrically connects an end of a gate electrode or a gate wire connected to this thin film transistor to a field made to remain in the state of said metal thin film, A process of forming an oxide film on anode in a gate electrode of said thin film transistor, or the surface of a gate wire by using as a voltage impressing terminal a field made remaining in the state of said metal thin film.

[Claim 9]They are some gate electrodes or gate wires which are connected to said thin film transistor, A manufacturing method of a semiconductor device of an application for patent having

the process of forming a gate electrode or a gate wire which established an anodization control means which controls advance of anodization of a gate electrode or a gate wire in a position of said voltage impressing terminal slippage given in the 8th paragraph of a range.
[Claim 10]They are some gate electrodes or gate wires which are connected to said thin film transistor, An anodization control means which controls advance of anodization of said gate electrode or a gate wire in a position of said voltage impressing terminal slippage is established. And a manufacturing method of a semiconductor device of an application for patent having the process of forming a gate electrode or a gate wire which provided the 2nd voltage impressing terminal that branched from a position of said thin film transistor slippage rather than this anodization control means given in the 8th paragraph of a range.
[Claim 11]A manufacturing method of a semiconductor device characterized by comprising the following.
A process of depositing a metal thin film on a substrate which has an insulation surface.
A process of making a partial area of this metal thin film remaining in the state of a metal thin film, and forming a metal electrode.
A process of oxidizing other fields of said metal thin film thoroughly, and forming a metallic oxide film.
On this metallic oxide film, semiconductor membrane and a process of depositing gate dielectric film and forming two or more thin film transistors on said substrate further, A process of forming a contact hole in said gate dielectric film on said metal electrode, A process of being in gate electrode **** of one thin film transistor among said two or more thin film transistors, and electrically connecting a gate wire to said metal electrode via said contact hole, A process of forming an oxide film on anode in a gate electrode of two or more of said thin film transistors, or the surface of a gate wire. A process of depositing an interlayer insulation film on said two or more thin film transistors, and a process of forming a contact hole in this interlayer insulation film and said gate dielectric film on said metal electrode, A process of electrically connecting at least one of said two or more thin film transistors of a source electrode of others and a thin film transistor, or a drain electrode to said metal electrode via said contact hole.

[Claim 12]The 7th paragraph of a range of an application for patent thru/or a manufacturing method of a semiconductor device given in the 11th paragraph having the process of forming said metallic oxide film by oxidizing a metal thin film deposited on said substrate using an anode oxidation method or a thermal oxidation method.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]Especially this invention relates to a thin film transistor used for an active matrix type liquid crystal display device or its circumference drive circuit, and a manufacturing

method for the same about a thin film transistor.
[0002]
[Description of the Prior Art]In recent years, the active matrix type liquid crystal display device attracts attention as a display which has an advantage of a light weight and low power consumption with a thin shape. Also in it, it has a great hope for the art which forms the thin film transistor (the following TFT is called.) which uses a polycrystalline silicon thin film as a liquid crystal driver element on a cheap low melting point glass substrate from the demand of large-area-izing, high-resolution-izing, low-cost-izing, etc.
[0003]In such TFT using the polycrystalline silicon thin film as an active region of TFT, it has been an important technical problem to reduce the leakage current at the time of OFF. "Offset gate structure" is known as a method of reducing the leakage current at the time of this OFF. That is, an offset region is formed so that the source region and the drain area which were formed in the gate electrode and polycrystalline silicon thin film of TFT may not lap. Since the characteristic of TFT is greatly influenced by the width of this offset region, when forming TFT, to control the width of an offset region by high accuracy is needed.
[0004]Metallic materials, such as aluminum, are used for the gate electrode of TFT, an oxide film on anode is formed in that electrode surface, and the composition which makes an offset region a part for the thickness of this oxide film is known for the former as indicated by JP,5-267666,A. In this anodization process, as indicated by JP,6-338612,A, The method of reconciling formation of an offset region and electric insulating improvement is known by forming the oxide film on anode of the porosity which can be formed in the side of a gate electrode on comparatively low voltage, and forming the oxide film on anode of the quality of nonporous for making insulation with upper wiring good especially in the upper surface of a gate electrode.
[0005]
[Problem(s) to be Solved by the Invention]According to the above-mentioned conventional method, various advantages, such as prevention of degradation of an improvement of the corrosion resistance of an electrode, a hillock, etc. and electric insulating improvement, can be acquired by forming an oxide film on anode in the surface of the gate electrode of TFT. On the other hand, there was a problem shown below in the anodization process for obtaining an oxide film on anode on the surface of a gate electrode.
[0006]Usually, the substrate 100 in which the circuit pattern was formed is immersed into an electrolysis solution, and anodization is performed by impressing the voltage of minus to the substrate 101 which counters this substrate with positive voltage and this, as shown in drawing 8 (a). Generally, platinum with little degradation, etc. are used for the substrate 101 which counters in many cases. As shown in drawing 8 (b), the clip for voltage impressing, etc. are attached to the substrate 100 in which the circuit pattern was formed, and it is immersed into an electrolysis solution to the portion which is going to form an oxide film on anode.
[0007]When it is going to form the oxide film of shape which is different, respectively on the side and the upper surface of a gate electrode which comprised metal which uses aluminum as the main ingredients like the above-mentioned conventional example, it is necessary to anodize twice separately. In order to anodize only the side of a gate electrode effectively first, the resist pattern used on the occasion of etching of a gate electrode is made to act on the upper surface of the gate electrode which does not need anodization at the beginning as a mask in detail. Next, in order to anodize the gate electrode upper surface, the voltage impressing terminal for attaching to some gate electrodes the clip etc. which impress the voltage for anodization is needed, but. Some resist patterns which are the masks at the time of anodization were conventionally removed using methods, such as wiping off with a solvent, and the portion used as a voltage impressing terminal was secured.
[0008]Such a process of wiping off a resist pattern with a solvent, Sputtering, such as a metal thin film in the manufacturing process of the usual TFT, the stage film formation using a film deposition system called deposition, Or since the photolitho step using the developers and etching devices of an electrode, wiring, etc., such as patterning and etching, is a heterogeneous process, For example, when it was going to process mechanically, a special manufacturing installation which is not used by the manufacturing process of the usual TFT newly had to be

introduced, and an excessive investment was required. For this reason, only the process of wiping off a resist pattern with a solvent had to be processed by handicraft. However, in the process of wiping off a resist pattern manually, manufacturing efficiency fell remarkably and also the fault of carrying out yield lowering by the dust generated during work was produced.
[0009]In addition, in order to control by high accuracy the width of the offset region which influences the charactoristic of TFT greatly in an anodization process. There was fault that the voltage at the time of energization, current, and time needed to be controlled precise, and moreover the degrees of production showed dispersion by degradation of a solution etc. at the thickness of an oxide film on anode.
[0010]In the case of the liquid crystal display of a drive circuit integral type in which the transistor for pixels and the transistor for a drive which drives the transistor for pixels were formed on the same substrate. In order to raise clock frequency, the big transistor characteristics of the ON state current are required for the transistor for a drive, and on the other hand, the low transistor characteristics of the OFF state current are required for the transistor for pixels. So, with the transistor for a drive, width of the offset region was shortened, with the transistor for pixels, it was preferred to lengthen width of an offset region and the width of several kinds of offset regions was needed according to the purpose of using a transistor on the same substrate. for this reason, the thing for which the voltage impressing terminal for anodization is divided for every width of several kinds of offset regions, and the voltage and current at the time of each energization are changed in the former, or resistance welding time is changed -- thickness of an oxide film on anode -- not controlling -- it did not obtain but very complicated work was needed.
[0011]It is necessary to electrically connect N channel TFT and P channel TFT in the case of the liquid crystal display of a drive circuit integral type, and to constitute a circumference drive circuit in it. For example, when an Al film is used for the gate electrode of N channel TFT or P channel TFT, it is necessary to etch the oxide film on anode using phosphoric acid or fluoric acid. However, since the selection ratio of an oxide film on anode and the Al film which is the gate electrodes of a ground is very small in such etching, it is difficult to remove only an oxide film on anode by etching. Therefore, it was not easy to remove thoroughly the oxide film on anode formed in the surface of the gate electrode of TFT, and to secure the contact part for connection. Therefore, the problem that connection between N channel TFT and P channel TFT was not made good had arisen.
[0012]When this invention solves the above-mentioned technical problem, an oxide film on anode is formed with an anode oxidation method on the surface of a gate electrode and an offset region is formed, A special process is not needed, but an oxide film on anode can be formed by an easy process, and the width of two or more offset regions can be controlled with high precision, It aims at providing TFT which can obtain good contact to the transistor for pixels, and the transistor for a drive which drives it, and a manufacturing method for the same.
[0013]
[Means for Solving the Problem]A metallic oxide film field in which a semiconductor device of this invention oxidized selectively and formed a metal thin film formed on a substrate which has an insulation surface, It has a metal electrode formed in said some of metal thin films, and two or more thin film transistors formed on said metallic oxide film, and is characterized by electrically connecting this thin film transistor to said metal electrode, and the above-mentioned purpose is attained by that.
[0014]A metallic oxide film field which oxidized selectively and formed a metal thin film in which a semiconductor device of this invention was formed on a substrate which has an insulation surface, Have a metal electrode formed in said some of metal thin films, and two or more thin film transistors formed on said metallic oxide film, and a gate electrode of this thin film transistor or an end of a gate wire is electrically connected to said metal electrode, and, It is characterized by this metal electrode being a voltage impressing terminal at the time of anodizing a gate electrode or a gate wire of said thin film transistor, and the above-mentioned purpose is attained by that.
[0015]An anodization control means which is some of said gate electrodes or gate wires, and

controls advance of anodization of said gate electrode or a gate wire in a position of said voltage impressing terminal slippage may be established.

[0016]It is desirable to electrically connect with said gate wire the 2nd voltage impressing terminal that estranged with said voltage impressing terminal and was formed in a position of said thin film transistor slippage rather than said anodization control means.

[0017]A metallic oxide film field in which a semiconductor device of this invention oxidized selectively and formed a metal thin film formed on a substrate which has an insulation surface, A metal electrode which was made to remain without oxidizing said some of metal thin films, and was formed, Have two or more thin film transistors formed on said metallic oxide film, and among these thin film transistors At least one of a source electrode of one thin film transistor, or the drain electrodes. It is characterized by a gate electrode of other thin film transistors electrically being connected by relay electrode by said metal electrode, and the above-mentioned purpose is attained by that.

[0018]Said metal thin film is desirable metal in which anodization or thermal oxidation is possible, and is an oxide film on anode or an oxidizing film by metal which said metallic oxide film oxidizes [this anodization or] thermally.

[0019]A process of depositing a metal thin film on a substrate with which a manufacturing method of a semiconductor device of this invention has an insulation surface, A process of making a partial area of this metal thin film remaining in the state of a metal thin film, and oxidizing and using other fields as a metallic oxide film, The above-mentioned purpose is attained by that including an electrically connected process to a process of forming a thin film transistor on this metallic oxide film, and a field which made an electrode connected to this thin film transistor, or an end of wiring remain in the state of said metal thin film.

[0020]A process of forming an oxide film on anode in a gate electrode of said thin film transistor or the surface of a gate wire by using as a voltage impressing terminal a field made remaining in the state of said metal thin film may also be included.

[0021]It is some gate electrodes or gate wires which are connected to said thin film transistor, and it is desirable to include a process of forming a gate electrode or a gate wire which established an anodization control means which controls advance of anodization of a gate electrode or a gate wire in a position of said voltage impressing terminal slippage.

[0022]They are some gate electrodes or gate wires which are connected to said thin film transistor, An anodization control means which controls advance of anodization of said gate electrode or a gate wire in a position of said voltage impressing terminal slippage is established, And a process of forming a gate electrode or a gate wire which provided the 2nd voltage impressing terminal that branched from a position of said thin film transistor slippage rather than this anodization control means may also be included.

[0023]A process of depositing a metal thin film on a substrate with which a manufacturing method of a semiconductor device of this invention has an insulation surface, A process of making a partial area of this metal thin film remaining in the state of a metal thin film, and forming a metal electrode, A process of oxidizing other fields of said metal thin film thoroughly, and forming a metallic oxide film, On this metallic oxide film, semiconductor membrane and a process of depositing gate dielectric film and forming two or more thin film transistors on said substrate further, A process of forming a contact hole in said gate dielectric film on said metal electrode, A process of being in gate electrode **** of one thin film transistor among said two or more thin film transistors, and electrically connecting a gate wire to said metal electrode via said contact hole, A process of forming an oxide film on anode in a gate electrode of two or more of said thin film transistors, or the surface of a gate wire, A process of depositing an interlayer insulation film on said two or more thin film transistors, and a process of forming a contact hole in this interlayer insulation film and said gate dielectric film on said metal electrode, The above-mentioned purpose is attained by that including a process of electrically connecting at least one of said two or more thin film transistors of a source electrode of others and a thin film transistor, or a drain electrode to said metal electrode via said contact hole.

[0024]A process of oxidizing a metal thin film deposited on said substrate using an anode oxidation method or a thermal oxidation method, and forming said metallic oxide film may be

included.
[0025]Hereafter, an operation of the above-mentioned composition is explained.
[0026]According to this invention, TFT is formed on a metallic oxide film which a metal thin film formed on a substrate was oxidized, and was formed, and it is constituted so that a gate electrode or a gate wire of TFT may be connected to a voltage impressing terminal by a field made to remain while it has been a metal thin film. Therefore, since it becomes unnecessary to pass through a special process of exfoliating in some masks used for patterning of a gate electrode when forming an oxide film on anode in the surface of a gate electrode, especially the side of a gate electrode, a process of forming an oxide film on anode in the surface of a gate electrode, especially the side of a gate electrode becomes simple.
[0027]By an anodization control means, delicate control of voltage at the time of anodization, current, and time becomes unnecessary, and it becomes very easy to form an oxide film on anode of desired thickness in the surface of a gate electrode. And it becomes possible by using two or more kinds of anodization control means to form an oxide film on anode of two or more kinds of thickness at an anodization process once. That is, in the same board, TFT which has two or more kinds of offset regions can be formed.
[0028]When two or more TFT(s) in which an oxide film on anode was formed on the surface of a gate electrode are connected mutually, On a substrate, a field made to remain with a metal thin film is used as a relay electrode, and at least one of a source electrode of one TFT and the drain electrodes and a gate electrode of other TFT(s) are electrically connected via the aforementioned relay electrode among two or more TFT(s). As a result, since it becomes unnecessary to perform a process of carrying out etching removal of the oxide film on anode currently formed in the surface of a gate electrode of two or more TFT(s), good contact can be obtained.
[0029]Since a voltage impressing terminal and a relay electrode which are formed with these metal thin film form simultaneously when they oxidize a metal thin film formed on a substrate and form a metallic oxide film, an unnecessary level difference by having formed a voltage impressing terminal and a relay electrode does not produce them.
[0030]
[Embodiment of the Invention]Hereafter, an embodiment of the invention is described.
[0031](Embodiment 1) Drawing 1 (a) is a top view of the substrate in which TFT of this embodiment and the voltage impressing terminal for anodization were formed. Drawing 1 (b) is a sectional view of the portion shown by the A-A' line of drawing 1 (a), and drawing 1 (c) is a sectional view of the portion shown by the B-B' line of drawing 1 (a). Drawing 1 (a) In - (c), the metallic oxide film 2 which oxidized and formed the metal thin film on the insulating substrate 1 is formed, the polycrystalline silicon thin film 3 is patterned after island shape, and the gate dielectric film 4 is formed on it. The gate dielectric film 4 is processed so that the field made to remain as a metal thin film, without oxidizing, i.e., the portion used as the voltage impressing terminal 5 for anodization, may be exposed. On the gate dielectric film 4, the gate wire 6a and the gate electrode 6b are formed, and it is electrically connected to the voltage impressing terminal 5. The mask pattern at the time of patterning the gate wire 6a and the gate electrode 6b on the gate wire 6a and the gate electrode 6b is left behind, and this serves as the mask 7 at the time of anodization.
[0032]The top view in which - (e) shows the details of the manufacturing method of this invention, and drawing 2 (a) drawing 2 (f) - (j) are the sectional views of the portion shown by the C-C' line of drawing 2 (a) - (e), respectively. A metal thin film is made to deposit by sputtering process etc. all over the insulating substrates 1, such as a quartz substrate or a glass substrate, first, as shown in drawing 2 (a) and (f). As a metal thin film, the metal which makes the main ingredients aluminum, Ta, Ti, Nb, or these can be used. In this embodiment, Ta thin film was used as a metal thin film. Since trouble is to form a metallic oxide film when the thickness of Ta thin film is too thick although what is necessary is just to determine the thickness of Ta thin film suitably in consideration of the method of forming a metallic oxide film, or its condition, About 100-200 nm was made to deposit on a substrate in about 100-150-nm thickness preferably at this embodiment.

[0033]Then, the mask 7 was formed in the field which serves as the voltage impressing terminal 5 for anodization after on Ta thin film, the other field of Ta thin film was oxidized, and the metallic oxide film 2 was formed. After the mask 7 provided on the metal thin film forms the metallic oxide film 2, it is removed. As a method of oxidizing Ta thin film and forming a metallic oxide film, an anode oxidation method and a thermal oxidation method can be used.

[0034]When forming a metallic oxide film with an anode oxidation method, the substrate in which Ta thin film was formed into electrolysis solutions, such as ammonium borate and ammonium tartrate, can be immersed, voltage can be impressed between the negative poles in the same electrolysis solution by the ability to make this into the anode, and Ta thin film in an electrolysis solution can be oxidized. Since the thickness and impressed electromotive force of an oxide film have proportionality, they should just determine anodization conditions, such as impressed electromotive force, in consideration of the thickness of Ta thin film.

[0035]When forming a metallic oxide film by a thermal oxidation method, it can be made to oxidize by heating the substrate in which Ta thin film was formed, at about 500 ** in oxygen environment. Since the thickness and cooking temperature of an oxide film have proportionality, they should just determine thermal oxidation conditions, such as cooking temperature, in consideration of the thickness of Ta thin film.

[0036]The mask provided on a metal thin film should just be construction material which bears an anodization process, when using an anode oxidation method, and polyimide, photosensitive polyimide, etc. can be used for it. It can use, when the photoresist used by the usual photolitho step also processes the surface of a metal thin film. Since patterning by the usual photolitho step is easy for photoresist, photosensitive polyimide, etc., they are suitable for forming the voltage impressing terminal 5 in desired shape. When using a thermal oxidation method, it is appropriate to pattern a SiO_2 film after predetermined shape and to use it for a mask, for example, since heat resistance is required.

[0037]Next, as shown in drawing 2 (b) and (g), the pattern of the island shape by the polycrystalline silicon thin film 3 is formed on the metallic oxide film 2. A way the polycrystalline silicon thin film 3 forms a polycrystalline silicon thin film directly with a CVD method etc. on a metallic oxide film in this invention, Or even if it forms the solid phase grown method or laser beam heat-treated and crystallized at the temperature of about 600 ** using which method of the laser crystallization method made to glare and fuse and recrystallize after forming an amorphous silicon thin film with plasma CVD method etc., it does not interfere. In this embodiment, the amorphous silicon thin film was made to deposit in about 50-100-nm thickness on a substrate, it irradiated with the laser beam, and the method of crystallizing an amorphous silicon thin film was used.

[0038]As a laser beam to be used, a XeCl excimer laser (wavelength of 308 nm), a KrF excimer laser (wavelength of 248 nm), an ArF excimer laser (wavelength of 193 nm), a XeF excimer laser (wavelength of 353 nm), etc. can be used. A laser beam can be glared from any direction of a surface [in which the amorphous silicon thin film of the insulating substrate was formed] side, or other surface, i.e., rear face of insulating substrate, side. However, to irradiate with a laser beam from the rear-face side of an insulating substrate, it is necessary to take into consideration the loss by absorption of the laser beam by an insulating substrate. In this case, if an insulating substrate is a quartz substrate, absorption of the laser beam by a substrate is slight, but. Since absorption of the laser beam by a substrate takes place depending on the wavelength of a laser beam in using a low melting point glass substrate, it is desirable to use a XeCl excimer laser with comparatively little absorption, a XeF excimer laser, etc.

[0039]If it irradiates with a laser beam from the rear-face side of an insulating substrate, the effect of avoiding the adverse effect of the surface of semiconductor membrane carrying out surface roughening, or unevenness occurring is expectable. The exposure conditions of a laser beam change with the membraneous quality of the film with which a laser beam is irradiated, thickness, etc. In this embodiment, it irradiated with the laser beam from the surface [in which the amorphous silicon thin film of the insulating substrate was formed] side, and the energy density of the laser beam was made into 200 - 400 mJ/cm^2, for example, a 300 mJ/cm^2 grade.

In order to improve the homogeneity of a crystal at the time of a laser beam exposure, the substrate was heated at 200–300 ** or 400 **, for example, 400 **. A long side can process the shape of a laser beam into the long shape several centimeters – about ten cm or more than it, and whose shorter side are about several millimeters according to the optical system of a lens etc. from the spot form about several millimeter angle – several centimeter angle, and any laser beam can be used by this embodiment.

[0040]Then, the gate dielectric film 4 is formed by a vacuum CVD method or plasma CVD method over an entire substrate so that the polycrystalline silicon thin film 3 patterned after island shape may be covered. The SiO_2 film was made to deposit in about 100–nm thickness at this embodiment. The rear gate insulator layer 4 is processed so that the field used as the voltage impressing terminal 5 for anodization may be exposed.

[0041]Next, as shown in drawing 2 (c) and (h), it migrates to an entire substrate including the field used as the voltage impressing terminal 5 for anodization, the metal thin film used as a gate wire and a gate electrode accumulates, and the resist pattern for patterning a gate electrode on it is formed.

[0042]This resist pattern is used also as the mask 7 at the time of forming an oxide film on anode in the side of a gate electrode. Therefore, it is necessary to bear an anodization process and especially photosensitive polyimide is [polyimide etc.] suitable. It can use, if the photoresist used by the usual photolitho step also forms a thin oxide film in the surface of a metal thin film. As a metal thin film, the metal in which the main ingredients and ********** are possible can be used for aluminum, Ti, Nb, etc. In order to form low resistance electrode wiring especially, it is desirable to use the metal which uses aluminum, such as aluminum, AlSi, AlTi, and AlSc, as the main ingredients. The metal thin film used as a gate wire and a gate electrode was made to deposit aluminum using the metal thin film used as the main ingredients by about 300–500 nm, for example, 300 nm, thickness in this embodiment.

[0043]Next, as shown in drawing 2 (d) and (i), a resist pattern is used, a metal thin film is patterned and etched, and the gate wire 6a and the gate electrode 6b are formed. Thus, the gate wire 6a and the gate electrode 6b are electrically connected to the voltage impressing terminal 5 for anodization. Then, the porous oxide film on anode 8a is formed in the side of the gate electrode 6b by using this resist pattern as the mask 7. The porous oxide film on anode 8a is obtained by anodizing using electrolysis solutions, such as 3 to 20% of citrate, oxalic acid, phosphoric acid, and chromic acid. In this embodiment, the substrate was immersed in 10% of citrate, and it anodized by impressing the constant voltage of 10–50V, for example, the voltage of 10V, to the voltage impressing terminal 5.

[0044]Next, as shown in drawing 2 (e) and (h), the mask 7 is removed, the upper surface of the gate electrode 6b is exposed, and the oxide film on anode 8b of the quality of nonporous is formed. The oxide film on anode 8b of the quality of nonporous is obtained by anodizing using ethylene glycol solutions, such as 3 to 10% of tartaric acid, boric acid, and nitric acid. In this embodiment, it anodized by immersing a substrate in the ethylene glycol solution of 3% of tartaric acid, sending current through this, and raising voltage to 120V at per-minute 1–5V, for example, 4 v/m. After forming the porous oxide film on anode 8a in the side of the gate electrode 6b and forming the oxide film on anode 8b of the quality of nonporous in the upper surface, To the source region and the drain area 9 of the polycrystalline silicon thin film 3, ion implantation, When creating N channel transistor using a laser doping process or the plasma doping method and creating P^+ and P channel transistor, B^+ is doped and the channel regions 10 and the offset region 11 are formed. Then, an impurity is activated using methods, such as laser annealing, and the interlayer insulation film 12 is laminated. It is common to the interlayer insulation film 12 to laminate the SiO_2 film (hundreds of nm – several micrometers) by the plasma CVD method made from good organic Silang of step coverage nature etc. A silicon nitride film can also be used for others. At this embodiment, the SiO_2 film was laminated by about 300–nm thickness. Finally the opening of the contact hole 13 is carried out to the interlayer insulation film 12 and the gate dielectric film 4, and a source electrode and the drain electrode 14 are formed. Sauce and the drain electrode 14 are formed with metallic materials, such as aluminum.

[0045]As mentioned above, according to this embodiment, when forming an oxide film on anode in the circumference of the gate electrode 6b, it is not necessary to perform the process of removing some resist patterns used as the mask of anodization, and an oxide film on anode can be efficiently formed only using the manufacturing installation which is carrying out normal use.
[0046]Although this embodiment explained taking the case of the quartz substrate or an amorphous board like a glass substrate, crystalline substrates, such as sapphire and CaF_2, may be sufficient as a substrate. The process after forming an oxide film on anode in the circumference of the laser crystallization method in the above-mentioned manufacturing method and a gate electrode shows an example in the manufacturing method of TFT, and the manufacturing method of TFT of this invention is not limited to this.
[0047](Embodiment 2) Drawing 3 (a) is a top view of the substrate in which TFT of this embodiment and the voltage impressing terminal for anodization were formed. Drawing 3 (b) is a sectional view of the portion shown by the D-D' line of drawing 3 (a). A metal thin film is made to deposit by sputtering process etc. all over the insulating substrates 30, such as a quartz substrate or a glass substrate, first like Embodiment 1 in drawing 3 (a) and (b). In this embodiment, Ta thin film was used as a metal thin film. Since trouble is to form a metallic oxide film when the thickness of Ta thin film is too thick although what is necessary is just to determine the thickness of Ta thin film suitably in consideration of the method of forming a metallic oxide film, or its condition, About 100-200 nm was made to deposit on a substrate in about 100-150-nm thickness preferably at this embodiment.
[0048]Then, the mask was provided in the field which serves as the 1st voltage impressing terminal 31 for anodization after on Ta thin film, the other field of Ta thin film was oxidized, and the metallic oxide film 32 was formed. After the mask provided on the metal thin film forms the metallic oxide film 32, it is removed. As a method of oxidizing Ta thin film and forming a metallic oxide film, an anode oxidation method and a thermal oxidation method can be used. The method of oxidizing Ta thin film and forming a metallic oxide film should just use the same method as Embodiment 1. Then, the polycrystalline silicon thin film 33 is formed in island shape like Embodiment 1, and it is processed so that the field which deposits gate dielectric film and serves as the 1st voltage impressing terminal 31 for anodization may be exposed.
[0049]As shown in drawing 3 (a), the gate wire 34a and the gate electrode 35b are formed so that the voltage impressing terminal 31 may be touched. In that case, the anodization control means 35 is formed in voltage impressing terminal 31 slippage [the gate wire 34a] of the 1st, and the 2nd voltage impressing terminal 36 that branched from the position of TFT slippage rather than the anodization control 36 of the gate wire 34a is formed.
[0050]When the anodization control means 35 anodizes, if this portion serves as an oxide film thoroughly, it will make width of a circuit pattern thin so that energization may stop. What is necessary is just to determine suitably the width of the circuit pattern of this anodization control means 35 according to the width of a desired offset region. In this embodiment, they could be 1 micrometer - about 4 micrometers.
[0051]Then, it anodizes and a porous oxide film on anode is formed in the side of the gate electrode 35b. A porous oxide film on anode is obtained by anodizing using electrolysis solutions, such as 3 to 20% of citrate, oxalic acid, phosphoric acid, and chromic acid. In this embodiment, the substrate was immersed in 10% of citrate, and it anodized by impressing the constant voltage of 10-50V, for example, the voltage of 8V, to the 1st voltage impressing terminal 31. If voltage is impressed from the 1st voltage impressing terminal 31, anodization advances and the anodization control means 35 oxidizes thoroughly, the conductivity of the portion will be lost and anodization will stop in a previous portion from the anodization control means 35. That is, the porous oxide film on anode according to the width of the anodization control means 35 will be formed in the side of the gate electrode 35b. According to this embodiment, a porous oxide film on anode is formed in the side of the gate electrode 35b by a thickness of 500 nm - 2 micrometers.
[0052]Next, the mask 39 is removed and the upper surface of the gate electrode 35b is exposed. Then, voltage is impressed to the 2nd voltage impressing terminal 36, and the oxide film on anode of the quality of nonporous is formed in the upper surface of the gate electrode 35b. The oxide film on anode of the quality of nonporous is obtained by anodizing using ethylene glycol

solutions, such as 3 to 10% of tartaric acid, boric acid, and nitric acid. In this embodiment, it anodized by immersing a substrate in the ethylene glycol solution of 3% of tartaric acid, sending current through this, and raising voltage to 100V at per-minute 1-5V, for example, 4 v/m.
[0053]The 2nd voltage impressing terminal 36 has branched from the position of TFT slippage rather than the position in which the anodization control means 35 of the gate wire 34a was formed. Since voltage can be again impressed to the gate wire 34a and the gate electrode 35b which advance of anodization suspended by the anodization control means 35 by this, the oxide film on anode of the quality of nonporous can be formed in the upper surface of the gate electrode 35b. Hereafter, TFT is manufactured by the same process as Embodiment 1.
[0054]As mentioned above, when forming an oxide film on anode in the circumference of the gate electrode 34b according to this embodiment, It is not necessary to perform the process of removing some resist patterns used as the mask of anodization and also and since advance of anodization stops by the anodization control means 35 provided in some gate wires, delicate control of anodization conditions becomes unnecessary and the influence of degradation of solution etc. is reduced. Therefore, a complicated process like the conventional anodization process becomes unnecessary, and it can anodize easily. The oxide film on anode of the quality of nonporous can be formed in the upper surface of the gate electrode 34b with the 2nd voltage impressing terminal 36.
[0055](Embodiment 3) Drawing 4 (a) is a top view showing this embodiment. Drawing 4 (b) is a sectional view of the portion shown by the E-E' line of drawing 4 (a). Drawing 4 (c) is a sectional view of the portion shown by the F-F' line of drawing 4 (a). As shown in drawing 4 (a), oxidize Ta thin film made to deposit on a substrate, Ta thin film is made to remain in the metallic oxide film 32 and a position, it estranges with the 1st voltage impressing terminal 31 and the 1st voltage impressing terminal 31, and the 2nd voltage impressing terminal 36 is formed. Then, the polycrystalline silicon thin film 33 is formed in island shape, and it is processed so that the field which deposits gate dielectric film and serves as the 1st voltage impressing terminal 31 for anodization may be exposed. These processes are the same as that of Embodiment 1 and Embodiment 2.
[0056]Next, as shown in drawing 4 (b), it forms so that the gate wire 34a and the gate electrode 34b may electrically be connected to the 1st voltage impressing terminal 31. It provides in voltage impressing terminal 31 slippage of the 1st anodization control means 35 at the gate wire 34a. The gate wire 34a is connected with the 2nd voltage impressing terminal 36 via the contact hole 39 punctured by gate dielectric film, as shown in drawing 4 (c). The contact hole 39 is formed in the position of TFT slippage rather than the anodization control means 35. When the anodization control means 35 anodizes, if this portion serves as an oxide film thoroughly, it will make width of a circuit pattern thin so that energization may stop. What is necessary is just to determine suitably the width of the circuit pattern of this anodization control means 35 according to the width of a desired offset region. In this embodiment, they could be 1 micrometer - about 4 micrometers.
[0057]Then, it anodizes and a porous oxide film on anode is formed in the side of the gate electrode 34b. A porous oxide film on anode is obtained by anodizing using electrolysis solutions, such as 3 to 20% of citrate, oxalic acid, phosphoric acid, and chromic acid. In this embodiment, the substrate was immersed in 10% of citrate, and it anodized by impressing the constant voltage of 10-50V, for example, the voltage of 10V, to the 1st voltage impressing terminal 31. If voltage is impressed from the 1st voltage impressing terminal 31, anodization advances and the anodization control means 35 oxidizes thoroughly, the conductivity of the portion will be lost and anodization will stop in a previous portion from the anodization control means 35. That is, the porous oxide film on anode according to the width of the anodization control means 35 will be formed in the side of the gate electrode 34b. According to this embodiment, a porous oxide film on anode is formed in the side of the gate electrode 34b by a thickness of 500 nm - 2 micrometers.
[0058]Next, the mask 39 is removed and the upper surface of the gate electrode 34b is exposed. Then, voltage is impressed to the 2nd voltage impressing terminal 36, and the oxide film on anode of the quality of nonporous is formed in the upper surface of the gate electrode 34b. The

oxide film on anode of the quality of nonporous is obtained by anodizing using ethylene glycol solutions, such as 3 to 10% of tartaric acid, boric acid, and nitric acid. In this embodiment, it anodized by immersing a substrate in the ethylene glycol solution of 3% of tartaric acid, sending current through this, and raising voltage to 100V at per-minute 1-5V, for example, 4 v/m.

[0059]Rather than the position in which the anodization control means 35 of the gate wire 34a was formed, the 2nd voltage impressing terminal 36 is a position of TFT slippage, and is connected with the gate wire 34a via the contact hole 39 formed in gate dielectric film. Thereby, from the anodization control means 35, voltage can be again impressed to the gate wire 34a and the gate electrode 34b which advance of anodization suspended, and the oxide film on anode of the quality of nonporous can be formed in the upper surface of the gate electrode 34b. Hereafter, TFT is manufactured by the same process as Embodiment 1.

[0060]As mentioned above, since advance of anodization stops according to the thickness of the anodization control means 35 provided in some gate wires according to this embodiment, delicate control of anodization conditions becomes unnecessary and the influence of degradation of solution etc. is also reduced. Therefore, a complicated process like the conventional anodization process is unnecessary, and can anodize easily. If the 2nd voltage impressing terminal 36 is used after this, the oxide film on anode of the quality of nonporous can be formed in the upper surface of the gate electrode 34b.

[0061](Embodiment 4) Drawing 5 (a) is a top view showing this embodiment, Drawing 5 (b) is a sectional view of the portion shown by the G-G' line of drawing 5 (a). Drawing 5 (c) is a sectional view of the portion shown by the H-H' line of drawing 5 (a). As shown in drawing 5 (a), oxidize Ta thin film made to deposit on a substrate, Ta thin film is made to remain in the metallic oxide film 31 and a position, it estranges with the 1st voltage impressing terminal 31 and the 1st voltage impressing terminal 31, and the 2nd voltage impressing terminal 36 is formed. Then, the polycrystalline silicon thin film 33 is formed in island shape, and it is processed so that the field which deposits the gate dielectric film 38 and serves as the 1st voltage impressing terminal 31 for anodization may be exposed.

[0062]Next, it forms so that the gate wire 34a and the gate electrode 34b may electrically be connected to the 1st voltage impressing terminal 31. These processes are the same as that of Embodiment 1, Embodiment 2, and Embodiment 3. The portion which the 1st voltage impressing terminal 31 connected with the gate wire 34a and the gate electrode 34b serves as a gestalt as shown in drawing 5 (b). The anodization control means 35 is formed in voltage impressing terminal 31 slippage of the 1st at the gate wire 34a. As shown in drawing 5 (c), two or more gate wires 34a are connected with the 2nd voltage impressing terminal 36 via two or more contact holes 39 punctured by the gate dielectric film 33. The contact hole 39 is punctured by the position of TFT slippage rather than the anodization control 36.

[0063]When the anodization control means 35 anodizes, if this portion oxidizes thoroughly, it will make width of a circuit pattern thin so that energization may stop. What is necessary is just to determine suitably the width of the circuit pattern of this anodization control means 35 according to the width of a desired offset region. In this embodiment, they could be 1 micrometer - about 4 micrometers. Then, it anodizes and a porous oxide film on anode is formed in the side of the gate electrode 34b. The conditions of anodization are as having been shown in Embodiment 1. If voltage is impressed from the 1st voltage impressing terminal 31, anodization advances and the anodization control means 35 oxidizes thoroughly, the conductivity of the portion will be lost and anodization will stop in a previous portion from the anodization control means 35. That is, the porous oxide film on anode according to the width of the anodization control means 35 will be formed in the side of the gate electrode 34b. According to this embodiment, a porous oxide film on anode is formed in the side of the gate electrode 34b by a thickness of 500 nm - 2 micrometers. Next, the mask 37 is removed and the upper surface of the gate electrode 34b is exposed.

[0064]Then, voltage is impressed to the 2nd voltage impressing terminal 36, and the oxide film on anode of the quality of nonporous is formed in the upper surface of the gate electrode 34b. Rather than the position in which the anodization control means 35 of the gate wire 34a was formed, the 2nd voltage impressing terminal 36 is a position of TFT slippage, and is connected

with two or more gate wires 34a via the contact hole 39 punctured by the gate dielectric film 33. Voltage can be again impressed to two or more gate wires 34a and gate electrodes 34b which advance of anodization suspended by the anodization control means 35 by this, and the oxide film on anode of the quality of nonporous can be formed in the upper surface of the gate electrode 34b.

[0065]As mentioned above, since advance of anodization of the gate electrode 34b stops according to the thickness of the anodization control means 35 provided in some gate wires according to this embodiment, delicate control of anodization conditions becomes unnecessary and the influence of degradation of solution etc. is also reduced. In two or more gate wires, two or more oxide film thicknesses can be once obtained at an anodization process by providing the anodization control means of the width according to desired oxide film thicknesses in each gate electrode, respectively to form an oxide film on anode by two or more thickness.

[0066](Embodiment 5) Drawing 6 (a) is a top view showing this embodiment. Drawing 6 (b) is a sectional view of the portion shown by the I-I' line of drawing 6 (a).

[0067]Since circumference drive circuits, such as a liquid crystal display of a drive circuit integral type, are mainly constituted, TFT of this embodiment is used. TFT for circumference drive circuits consists of N channel TFT60 and P channelTFT61. As shown in drawing 6 (a) and drawing 6 (b), Ta thin film made to deposit on a substrate is oxidized, and the relay electrode 62 is formed in a position. N channelTFT60 and P channel TFT61 will electrically be connected via the relay electrode 62.

[0068]Next, the details of the manufacturing method of this invention are explained. The top view in which - (d) shows the details of the manufacturing method of this invention, and drawing 7 (a) drawing 7 (e) - (h) are the sectional views of the portion shown by the J-J' line of drawing 7 (a) - (d).

[0069]As shown in drawing 7 (a) and (e), Ta thin film made to deposit on a substrate is oxidized, and the metallic oxide film 63 and the relay electrode 62 are formed in a position. These formation methods are the same as that of other embodiments.

[0070]Next, as shown in drawing 7 (b) and (f), the polycrystalline silicon thin films 64n and 64p used as N channelTFT60 and P channel TFT61 which were shown in drawing 6 (a) and (b) are formed in island shape. The gate dielectric film 65 by a SiO_2 film etc. accumulates so that these polycrystalline silicon thin films 64n and 64p may be covered. Even if the formation method of a polycrystalline silicon thin film uses which well-known methods, such as a solid phase grown method and a laser crystallization method, it does not interfere.

[0071]Next, as shown in drawing 7 (c) and (g), the gate electrode 67n by the metal which makes aluminum the portion corresponding to the channel regions 66 of N channel TFT60 with the main ingredients is formed, The other end is electrically connected to the relay electrode 62 via the contact hole 68 punctured by the gate dielectric film 65. On the other hand, the gate electrode 67p is formed in the portion corresponding to the channel regions 66 of P channel TFT61 as well as N channel TFT60. The other end of this gate electrode 67p is connected to the wiring which is not illustrated. An oxide film on anode is formed in the surface of these gate electrodes 67n and 67p. Formation of an oxide film on anode can be performed by the method shown in Embodiment 4 from Embodiment 1. After oxide-film-on-anode formation, the gate electrode 67n is illustrating, after removing unnecessary wiring.

[0072]Next, as shown in drawing 7 (d) and (h), the source region and the drain areas 70n and 70p, and the offset regions 68n and 68p are formed in the polycrystalline silicon thin films 64n and 64p. The interlayer insulation film 71 accumulates on an entire substrate so that N channelTFT60 and P channel TFT61 may be covered. The source electrode and the drain electrode 72n of N channel TFT60 are connected to the source region and 70 n of drain areas of the polycrystalline silicon thin film 64n via the contact hole 68 punctured by the interlayer insulation film 71 and the gate dielectric film 65. On the other hand, the source electrode is electrically connected to the relay electrode 62 via the contact hole 68 punctured by the interlayer insulation film 71 and the gate dielectric film 65 among the source electrode of P channel TFT61, and the drain electrode 72p. Thus, N channelTFT60 and P channel TFT61 are electrically connected via the relay electrode 62.

[0073]As mentioned above, in [according to this embodiment] circumforonce drive circuits, such as a liquid crystal display of a drive circuit integral type mainly, When an oxide film on anode connects mutually N channel TFT and P channel TFT which were formed on the surface of a gate electrode, the process of carrying out etching removal only of the oxide film on anode formed on the surface of the gate electrode like before becomes unnecessary, and good contact can be obtained.
[0074]The above-mentioned manufacturing process shows an example in the manufacturing method of TFT, and the manufacturing method of TFT of this invention is not limited to this.
[0075]
[Effect of the Invention]Since the wiring of TFT or the end of an electrode currently formed on the metallic oxide film which oxidized some metal thin films made to deposit on a substrate is connected to the field made to remain with a metal thin film so that clearly from the above explanation, By using this field as a voltage impressing terminal or a relay electrode, the oxide film on anode was able to be easily formed in the gate electrode surface. When forming an oxide film on anode especially in the side of a gate electrode, it became unnecessary for example, to perform a special process like before, such as exfoliating in some masks used for patterning of a gate electrode.
[0076]Since the anodization control means provided and shone to some of gate electrodes or gate wires, delicate control of the voltage at the time of anodization, current, and time became unnecessary, and it became very easy to form the oxide film on anode of desired thickness in the surface of a gate electrode. Under the present circumstances, since the oxide film on anode of two or more kinds of thickness was once formed at the anodization process when using two or more kinds of anodization control means, it also became possible to form TFT which has two or more kinds of offset regions in the same board.
[0077]When connecting mutually two or more TFT(s) in which the oxide film on anode was formed on the surface of the gate electrode, it becomes unnecessary to have performed the process of carrying out etching removal of the oxide film on anode currently formed in the surface of the gate electrode of two or more TFT(s), good contact could be obtained, and the yield was able to be raised simultaneously.
[0078]This invention is an industrially useful invention which provides a highly efficient semiconductor device, the semiconductor device which comprises two or more highly efficient TFT(s) especially, or a semiconductor circuit as mentioned above.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1](a) is a top view showing Embodiment 1. (b) is a sectional view shown by an A-A' line, and a sectional view in which (c) is shown by a B-B' line.
[Drawing 2](a) The top view in which - (e) shows the manufacturing process of Embodiment 1, and (f) - (j) are sectional views shown by a C-C' line, respectively.

[Drawing 3](a) is a top view showing Embodiment 2. (b) is a sectional view shown by a D-D' line.
[Drawing 4](a) is a top view showing Embodiment 3. (b) is a sectional view shown by an E-E' line, and a sectional view in which (c) is shown by a F-F' line.
[Drawing 5](a) is a top view showing Embodiment 4. (b) is a sectional view shown by a G-G' line, and a sectional view in which (c) is shown by a H-H' line.
[Drawing 6](a) is a top view showing Embodiment 5. (b) is a sectional view shown by an I-I' line.
[Drawing 7](a) The top view in which - (d) shows the manufacturing process of Embodiment 5, and (e) - (h) are sectional views shown by a J-J' line, respectively.
[Drawing 8](a) - (b) is a key map showing an anode oxidation method.
[Description of Notations]
1 and 30 Insulating substrate
2, 32, and 63 Metallic oxide film
3, 33, 64n, 64p polycrystalline silicon thin film
4, 38, 65 gate dielectric film
5 Voltage impressing terminal
6a, 34a gate wire
6b, 34b, 67n, 67p gate electrode
7 and 37 Mask
8a A porous oxide film on anode
8b The oxide film on anode of the quality of nonporous
9 or 70 n, 70p source region, and a drain area
10, 66 channel regions
11 or 69 n, 69p offset region
12 and 71 Interlayer insulation film
13, 39, and 68 Contact hole
14 or 72 n, 72p source electrode, and a drain electrode
31 The 1st voltage impressing terminal
35 Anodization control means
36 The 2nd voltage impressing terminal
60 N channel TFT
61 P channel TFT
62 Relay electrode
100 The substrate in which the circuit pattern was formed
101 Counter substrate

[Translation done.]

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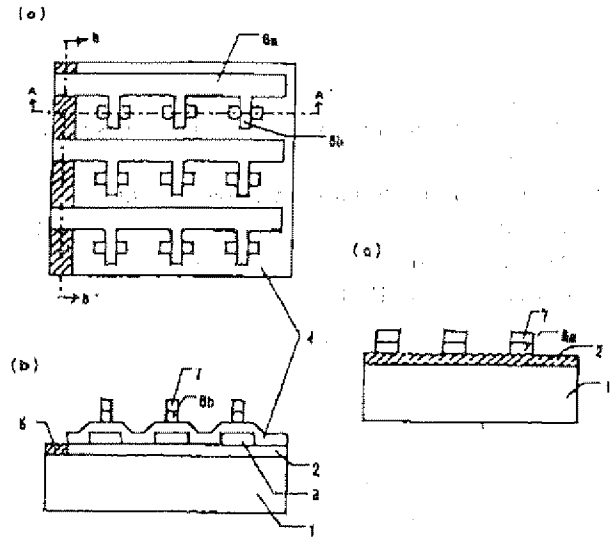
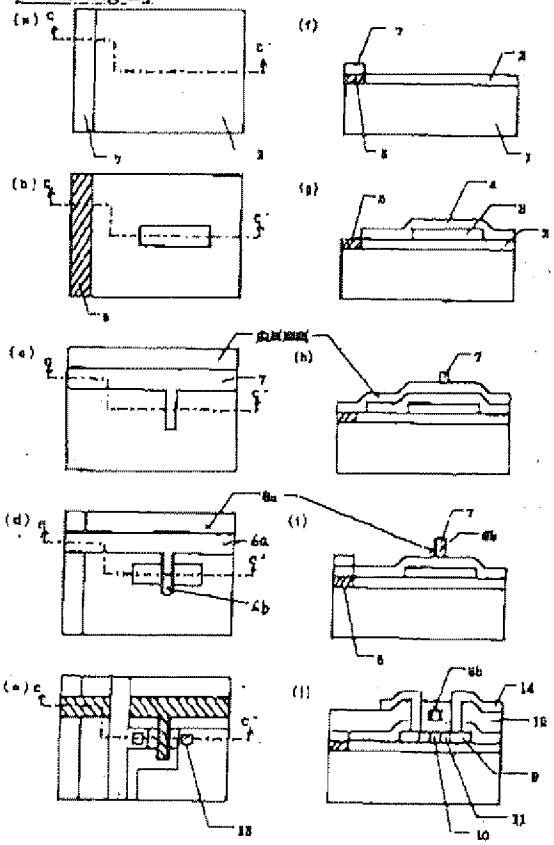
3.In the drawings, any words are not translated.

DRAWINGS

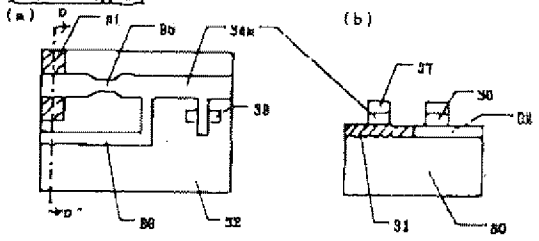
[Drawing 1]



[Drawing 2]



[Drawing 3]



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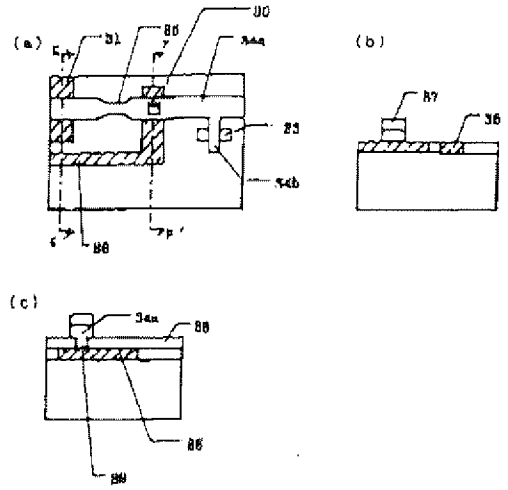
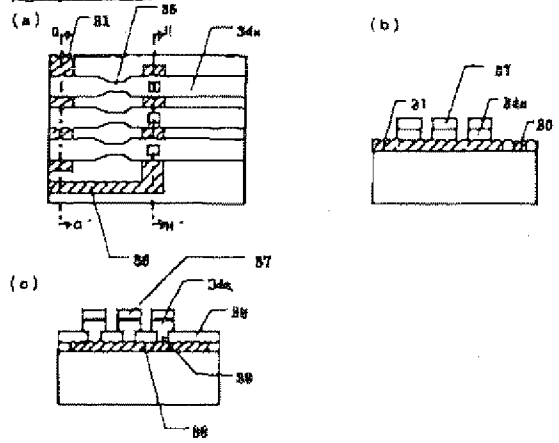
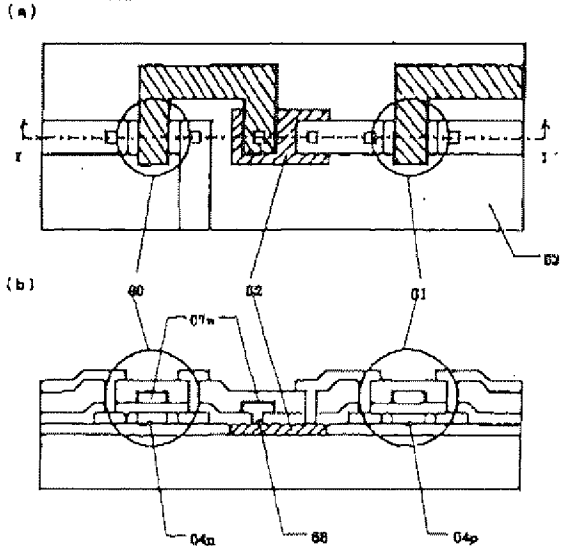


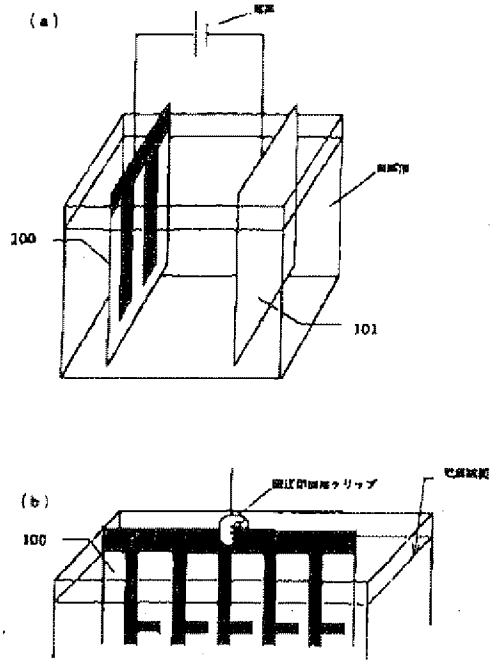
[Drawing 5]



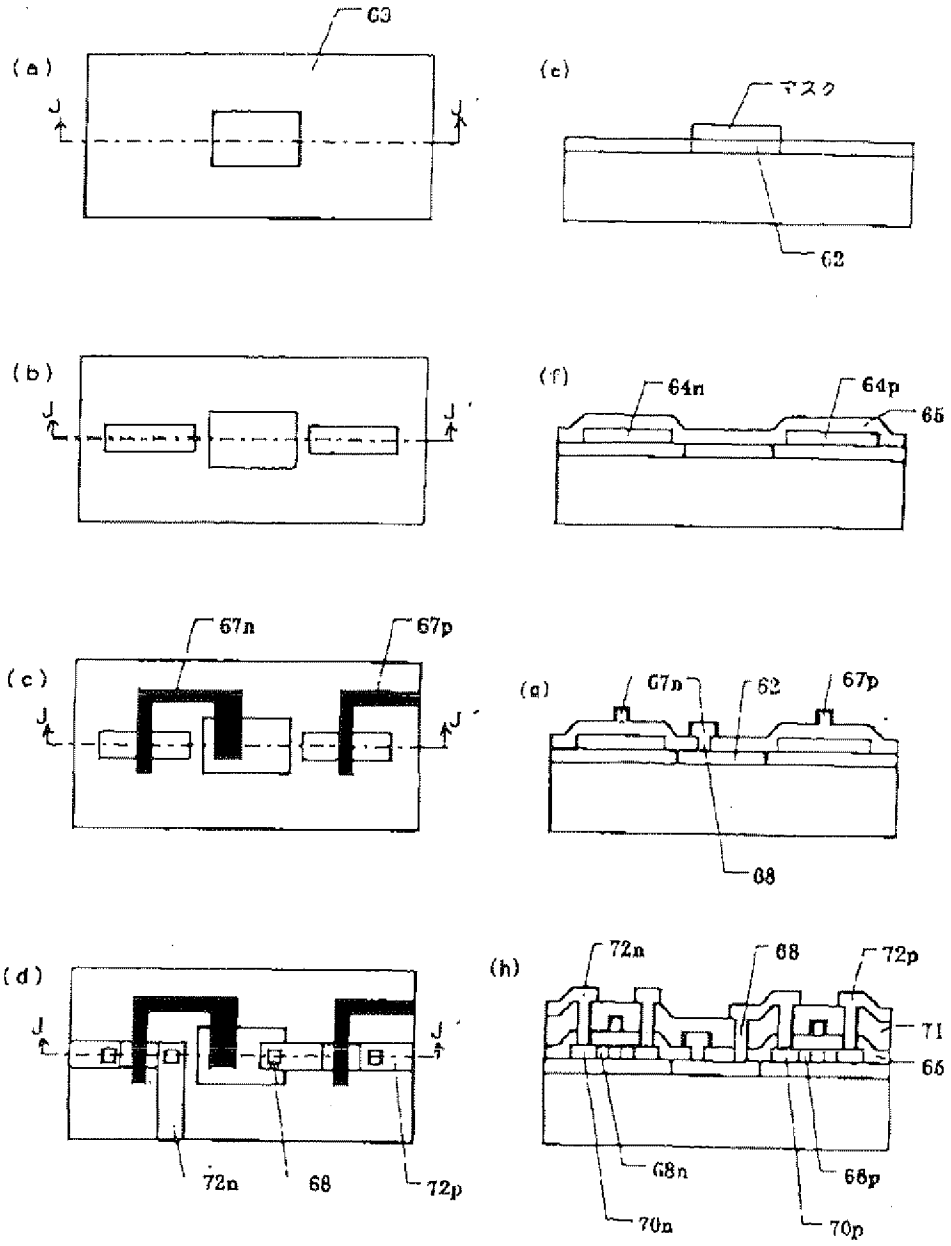
[Drawing 6]



[Drawing 8]



[Drawing 7]



[Translation done.]